# Bringing 3D Memory Cubes to Space: a "Rad-Hard by Design Study" with an Open Architecture, Phase II

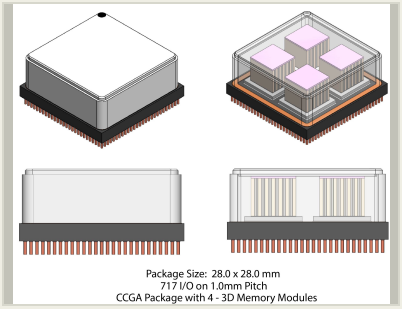
Completed Technology Project (2017 - 2021)

## Project Introduction

The computing capabilities of onboard spacecraft are a major limiting factor for accomplishing many classes of future missions. Although technology development efforts are underway that will provide improvements to spacecraft CPUs, they do not address the limitations of current onboard memory systems. In addition to CPU upgrades, effective execution of data-intensive operations such as terrain relative navigation, hazard detection and avoidance, autonomous planning and scheduling, and onboard science data processing and analysis require high-bandwidth, low-latency memory systems to maximize processor usage (the ?memory wall?) and provide rapid access to observational data captured by high-data-rate instruments (e.g., Hyperspectral Infrared Imager, Interferometric Synthetic Aperture Radar). 3D ICs, after a long wait, is now a reality. The first mainstream product is 3D memory cubes, where multiple memory tiers (4 DRAM tiers as of 2015) are vertically integrated to offer manifold improvement in size, capacity, speed, and power consumption compared with 2D counterparts. Indeed, these are the memory parts that will truly enable aforementioned missions. Unfortunately, none of these are ready for space. The purpose of this research is to investigate the challenges and opportunities in deploying 3D memory cubes into space missions.

## Anticipated Benefits

In order to effectively address the SWaP constraints of space hardware, it is desired to compact the electronics to as small a size as possible. Advances in the arena of 3D stacking and 3D ICs have opened a window of opportunity to integrate these types of packaging for space applications. Very high density, high bandwidth, RAD-hard reliable memory cubes would address some of the immediate needs for space applications. The one drawback is the ready availability of this type of space qualified 3D hardware. The proposed 3D RAD-hard memory stack will be directly applicable to space electronics requiring memory intensive applications. The technology derived from this study will allow NASA to utilize this on a broader range of capabilities that can be brought to space.Optimization of the logic base of any memory cube type has not been available for any application. Development of the design tools to achieve better optimization of these logic bases will in turn lead to a broader application base which will benefit not only the users for space applications, but will benefit terrestrial users to help improve the efficiency of their electronics by addressing SWaP issues.




Bringing 3D Memory Cubes to Space: a "Rad-Hard by Design Study" with an Open Architecture, Phase II Briefing Chart Image

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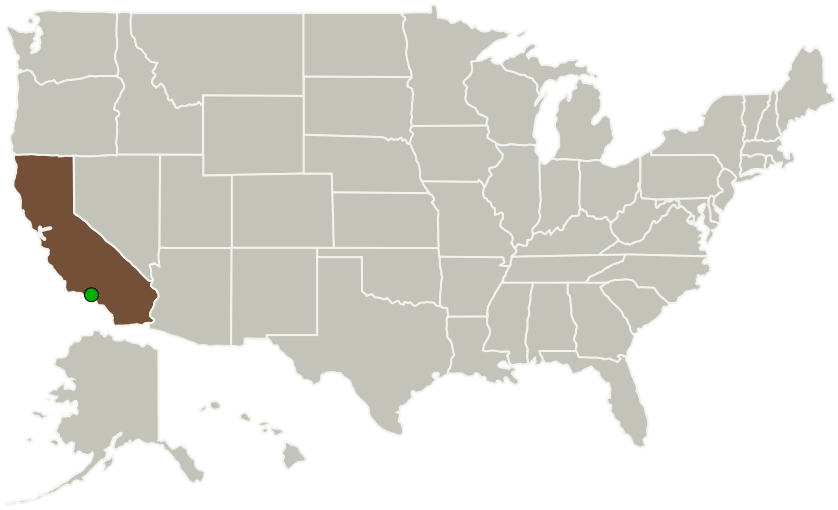

| Organizations Performing Work | Role | Type | Location |
|---|---|---|---|
| Irvine Sensors Corporation | Lead Organization | Industry | Costa Mesa, California |
| Jet Propulsion Laboratory(JPL) | Supporting Organization | NASA Center | Pasadena, California |

| Primary U.S. Work Locations |
|---|
| California |

## Organizational Responsibility

**Responsible Mission Directorate:**

Space Technology Mission Directorate (STMD)

**Lead Organization:**

Irvine Sensors Corporation

**Responsible Program:**

Small Business Innovation Research/Small Business Tech Transfer

## Project Management

**Program Director:**

Jason L Kessler

**Program Manager:**

Carlos Torrez

**Project Managers:**

Lynn M Torres
Carol R Lewis

**Principal Investigator:**

James Yamaguchi

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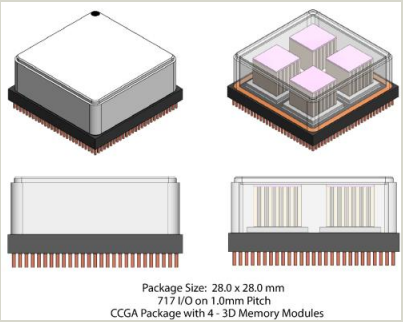
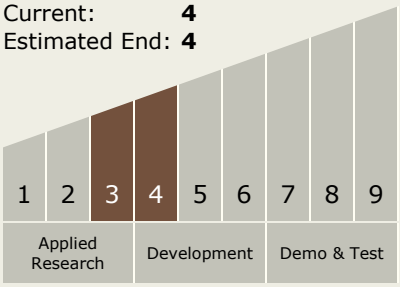
## Images




**Briefing Chart Image**
Bringing 3D Memory Cubes to Space: a "Rad-Hard by Design Study" with an Open Architecture, Phase II Briefing Chart Image *(https://techport.nasa.gov/image/133598)*

## Technology Maturity (TRL)

Start: **3**
Current: **4**
Estimated End: **4**




## Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System